

WHAT IS CLAIMED IS:

1. A fast Fourier transform (FFT) architecture, comprising:
2 a pipeline segment having a plurality of data-independent
3 pipelines that receive different time-domain data samples and
4 generate therefrom corresponding intermediate results; and
5 a parallel segment, coupled to all of said pipelines, that
6 receives said corresponding intermediate results and generates
7 therefrom corresponding frequency-domain results.

2. The architecture as recited in Claim 1 wherein each of
2 said plurality of data-independent pipelines receives a single
3 time-domain data sample at a time.

3. The architecture as recited in Claim 1 wherein each of
2 said data-independent pipelines is a radix-2² single-path delay
3 feedback pipeline.

4. The architecture as recited in Claim 1 wherein said
2 parallel segment is a radix-2 segment.

5. The architecture as recited in Claim 1 wherein a number
2 of said plurality of data-independent pipelines for a particular
3 application is based on both a time-domain data sample rate and a
4 clock rate pertaining to said application.

6. The architecture as recited in Claim 1 wherein a strength
2 reduction transformation is employed to substitute real multipliers
3 for complex multipliers.

7. The architecture as recited in Claim 1 wherein said
2 pipeline segment employs a hardware implementation.

8. A method of performing a fast Fourier transform (FFT),
comprising:

initially receiving different time-domain data samples into a plurality of data-independent pipelines of a pipeline segment, said data-independent pipelines generating therefrom corresponding intermediate results; and

subsequently receiving said corresponding intermediate results into a parallel segment coupled to all of said pipelines, said parallel segment generating therefrom corresponding frequency-domain results.

9. The method as recited in Claim 8 wherein each of said plurality of data-independent pipelines receives a single time-domain data sample at a time.

10. The method as recited in Claim 8 wherein each of said data-independent pipelines is a radix-2² single-path delay feedback pipeline.

11. The method as recited in Claim 8 wherein said parallel segment is a radix-2 segment.

12. The method as recited in Claim 8 wherein a number of said
2 plurality of data-independent pipelines for a particular
3 application is based on both a time-domain data sample rate and a
4 clock rate pertaining to said application.

13. The method as recited in Claim 8 wherein a strength
2 reduction transformation is employed to substitute real multipliers
3 for complex multipliers.

14. The method as recited in Claim 8 wherein said pipeline
2 segment employs a hardware implementation.

15. An Orthogonal Frequency Division Multiplex (OFDM)
2 receiver, comprising:
3 an input section that is coupled to a receive antenna;
4 a fast Fourier transform (FFT) section that is coupled to said
5 receive section, including:
6 a pipeline segment having a plurality of data-independent
7 pipelines that receive different time-domain data samples and
8 generate therefrom corresponding intermediate results, and
9 a parallel segment, coupled to all of said pipelines,
10 that receives said corresponding intermediate results and
11 generates therefrom corresponding frequency-domain results;
12 and
13 an output section that is coupled to said FFT section.

16. The receiver as recited in Claim 15 wherein each of said
2 plurality of data-independent pipelines receives a single time-
3 domain data sample at a time.

17. The receiver as recited in Claim 15 wherein each of said
2 data-independent pipelines is a radix-2² single-path delay feedback
3 pipeline.

18. The receiver as recited in Claim 15 wherein said parallel
2 segment is a radix-2 segment.

19. The receiver as recited in Claim 15 wherein a number of
2 said plurality of data-independent pipelines for a particular
3 application is based on both a time-domain data sample rate and a
4 clock rate pertaining to said application.

20. The receiver as recited in Claim 15 wherein a strength
2 reduction transformation is employed to substitute real multipliers
3 for complex multipliers.

21. The receiver as recited in Claim 15 wherein said pipeline
2 segment employs a hardware implementation.